WHAT IS CLAIMED IS:

1. A non-volatile memory comprising an array of memory cells, each memory cell having a source, a drain, a floating gate and a control gate, said floating gate receptive to variable amount of charges being stored therein for designating a plurality of memory states, said non-volatile memory further comprising:

predetermined voltages being applied respectively to the source, drain and control gate of a memory cell being sensed, thereby producing a source-drain current corresponding to the amount of charge stored in the floating gate of said memory cell being sensed, said source-drain current having an inherent noise fluctuation component; and

a sensing circuit connectable to said memory cell to measure an average value of said source-drain current over a predetermined period of time sufficient for the noise fluctuation component therein to cancel to a predetermined level.

2. A non-volatile memory as in claim 1, wherein said sensing circuit further comprises:

a current-to-frequency converter adapted to receive said source-drain current to produce an alternating signal, said alternating signal having a frequency that is related to said source-drain current; and

a counter to count the number of cycles of said alternating signal within said predetermined period of sensing time such that said amount of charged being stored on the floating gate or the source-drain current is determined from the number of cycles counted, thereby determining the corresponding memory state of said memory cell being sensed over said predetermined period of sensing time.

3. A non-volatile memory as in claim 2, wherein:

said predetermined period of sensing time is controlled by the time to count a predetermined number of cycles in an alternating signal produced by another current-to-frequency converter when sensing a reference current.

4. A non-volatile memory as in claim 2, wherein said sensing circuit further comprises:

a timing circuit for generating a sensing timing signal to enable said sensing circuit to sense said source-drain current over said predetermined period of sensing time.

5. A non-volatile memory as in claim 4, wherein said timing circuit further comprises:

a reference current source for providing a reference current;

a second current-to-frequency converter adapted to receive said reference current to produce a reference alternating signal; and

a second counter to count a number of cycles of said reference alternating signal; and wherein

said sensing timing signal is determined by the time to count a predetermined number of cycles in said reference alternating signal.

6. A non-volatile memory as in claim 5, wherein said reference current source is provided by the source-drain current of a reference memory cell whose floating gated is stored with a predetermined charge.

7. A non-volatile memory as in claim 1, wherein said sensing circuit further comprises:

a reference current from a reference current source for demarcating between two of said plurality of designated memory states;

an integrating comparator for sensing an average source-drain current of the memory cell being sensed relative to an average reference current over said predetermined period of time.

8. A non-volatile memory as in claim 7, wherein said integrating comparator includes a capacitor differential amplifier which further comprises:

a first capacitor coupled to said source-drain current of said memory cell such that a first voltage develops thereacross after said predetermined period of time, said first voltage being given substantially by the product of the capacitance of said first capacitor and said source-drain current integrated over said predetermined period of time;

a second capacitor similar to said first capacitor coupled to said reference current such that a second voltage develops thereacross after said predetermined period of time; and

a voltage comparator for comparing said first and second voltage, thereby determining the relative magnitudes of said source-drain current of said memory cell and said reference current.

9. A non-volatile memory as in claim 7, wherein said integrating comparator includes a switched capacitor differential amplifier.

10. A non-volatile memory as in claim 7, wherein said sensing circuit further comprises:

a first current mirror for reproducing said source-drain current of said memory cell into one or more scaled copies thereof; and

a second current mirror for reproducing said reference current into one or more scaled copies thereof,

thereby allowing one or more copies of said source-drain current of said memory cell and said reference current to be compared in parallel.

11. A non-volatile memory as in claim 10, wherein

said first current mirror is such that it reproduces said one or more scaled copies of said source-drain current of the memory cell that are substantially identical to each other; and

said second current mirror is such that it reproduces said one or more scaled copies of said reference current that are substantially in predetermined ratios of each other in accordance with a memory partitioning scheme of the memory cell.

12. A non-volatile memory as in claim 10, wherein

said first current mirror is such that it reproduces said one or more scaled copies of said source-drain current of the memory cell that are substantially in predetermined ratios of each other in accordance with a memory partitioning scheme of the memory cell; and

said second current mirror is such that it reproduces said one or more scaled copies of said reference current that are substantially identical to each other.

13. A non-volatile memory as in claims 1-12, wherein a plurality of memory cells is sensed in parallel.

14. A non-volatile memory as in claims 1-12, wherein said array of memory cells is EEPROM.

15. A non-volatile memory as in claims 1-12, wherein said array of memory cells is Flash EEPROM.

16. A non-volatile memory as in claims 1-12, wherein said plurality of designated states is two.

17. A non-volatile memory as in claims 1-12, wherein said plurality of designated states is greater than two.

18. In a non-volatile memory comprising an array of memory cells, each memory cell having a source, a drain, a floating gate and a control gate, said floating gate receptive to variable amount of charges being stored therein for designating a plurality of memory states, a method of sensing the memory state of a memory cell, comprising:

applying predetermined voltages respectively to the source, drain and control gate of said memory cell being sensed, thereby producing a source-drain current corresponding to the amount of charge stored in the floating gate of said memory cell being sensed, said source-drain current having an inherent noise fluctuation component; and

measuring an average value of said source-drain current over a predetermined period of time sufficient for the noise fluctuation component therein to cancel to a predetermined level.

19. A method of sensing the memory state of a memory cell as in 18, wherein said measuring include comparing said source-drain current with a reference current over said predetermined period of time.